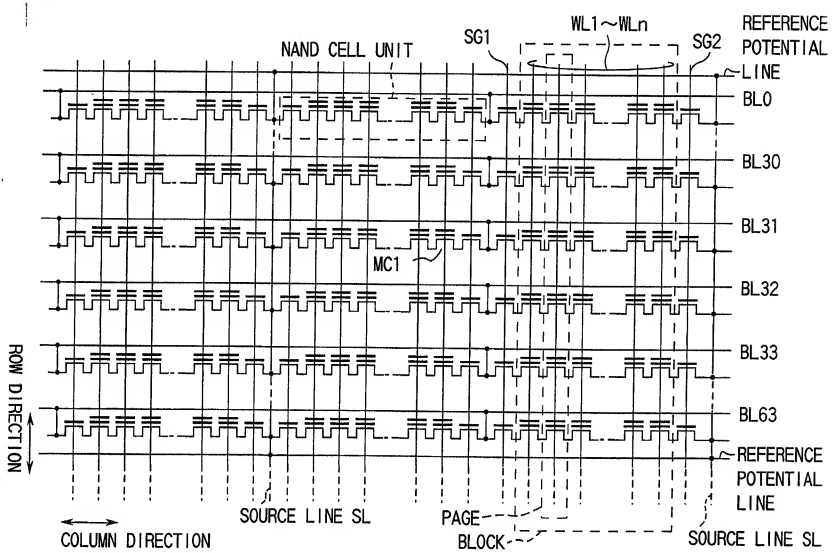


FIG. 1 PRIOR ART

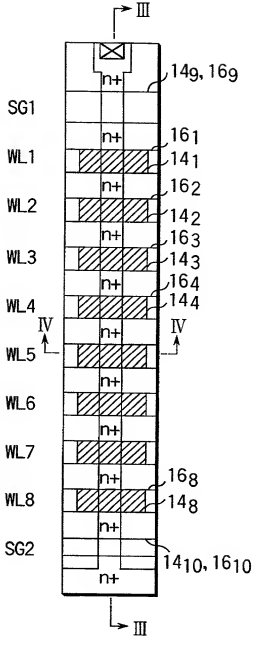


FIG. 2 PRIOR ART

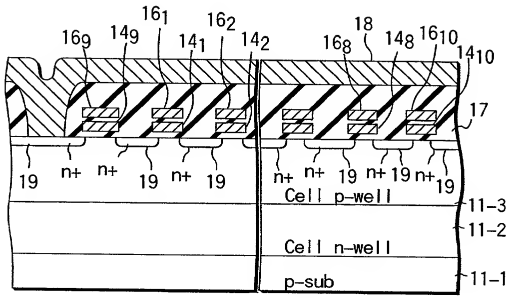


FIG. 3 PRIOR ART

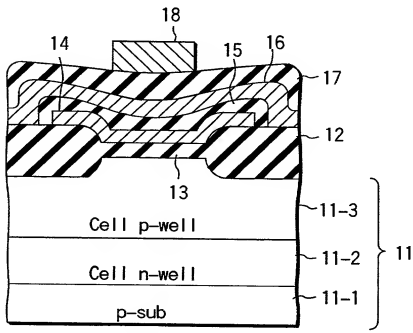


FIG. 4 PRIOR ART

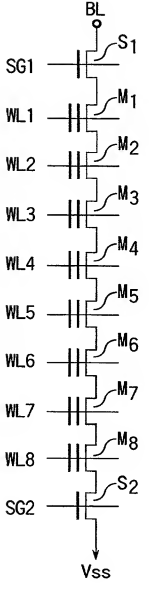


FIG. 5 PRIOR ART

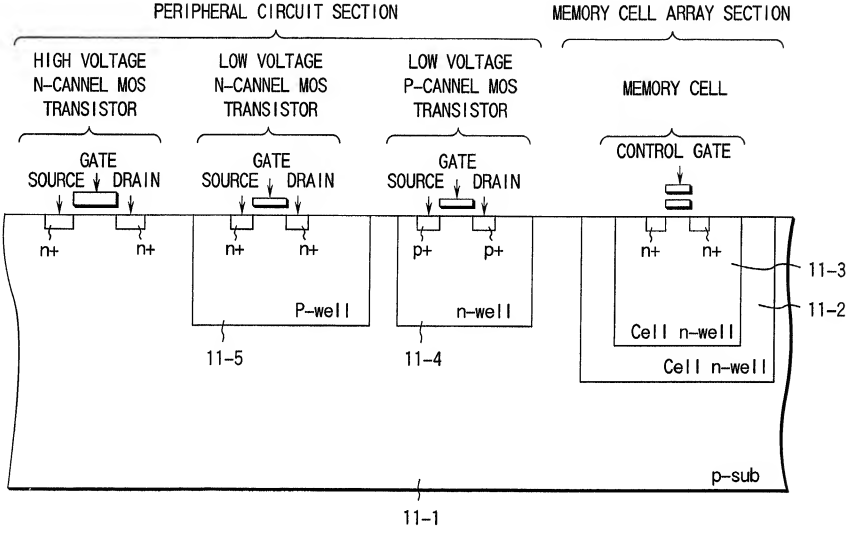


FIG.6 PRIOR ART

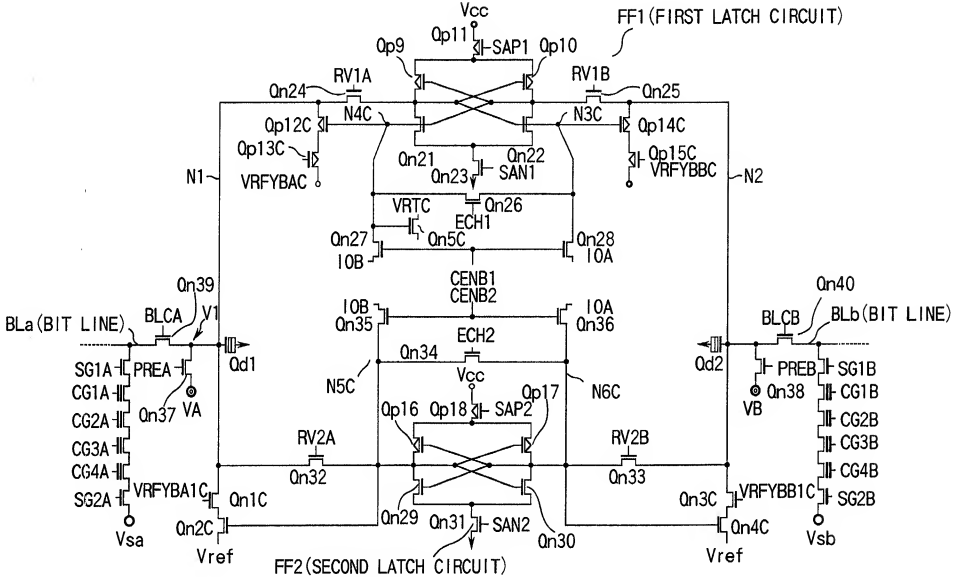


FIG. 7 PRIOR ART

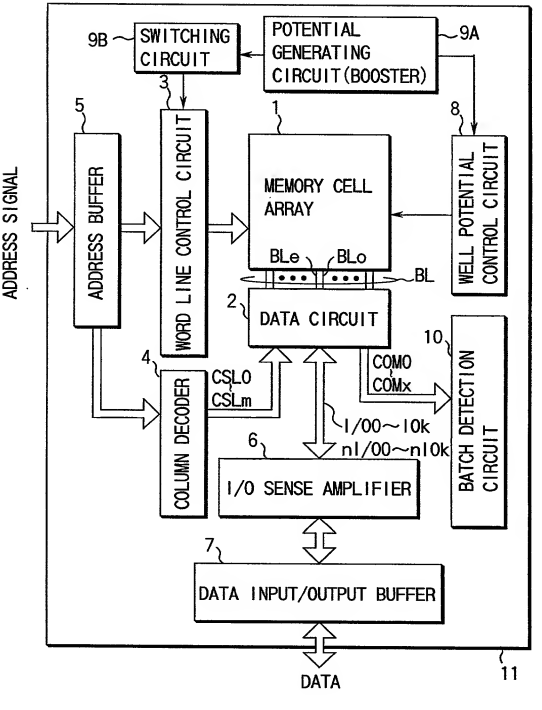

ADDRESS SIGNAL
9B
SWITCHING CIRCUIT
POTENTIAL GENERATING CIRCUIT(BOOSTER)
9A
3
5
1
8
ADDRESS BUFFER
WORD LINE CONTROL CIRCUIT
MEMORY CELL ARRAY
WELL POTENTIAL CONTROL CIRCUIT
BLe
BLo
BL
2
DATA CIRCUIT
10
4
CSL0
CSLm
COM0
COMx
COLUMN DECODER
I/00~I0k
nI/00~nI0k
6
I/O SENSE AMPLIFIER
BATCH DETECTION CIRCUIT
7
DATA INPUT/OUTPUT BUFFER
DATA
11

FIG. 8

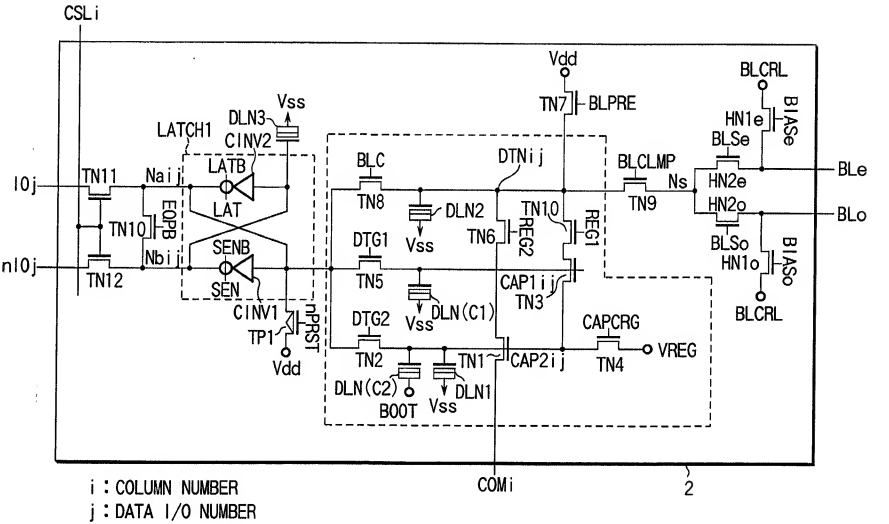


FIG. 9

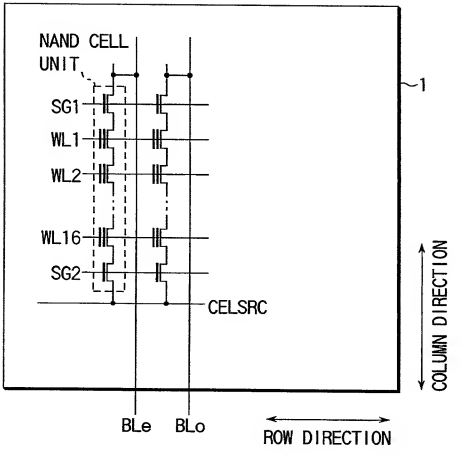

NAND CELL
UNIT
SG1
WL1
WL2
WL16
SG2
CELSRC
1
COLUMN DIRECTION
BLe
BLo
ROW DIRECTION

FIG. 10


CAk1
CBk2
CCk3
CSLi

FIG. 11

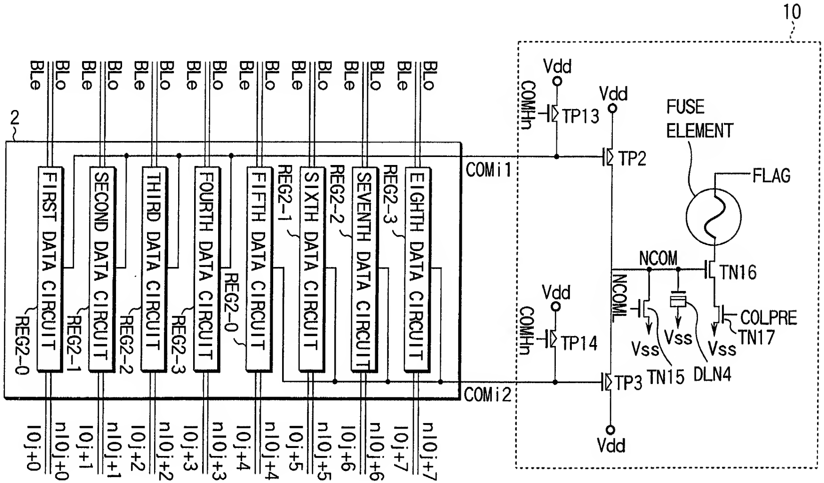
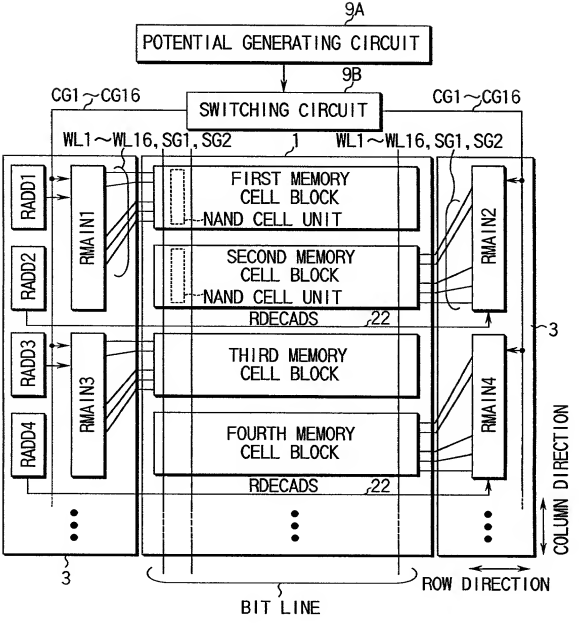

10
Vdd
COMHn
TP13
Vdd
TP2
FUSE
ELEMENT
FLAG
NCOM
TN16
NCOML
COLPRE
TN17
Vdd
COMHn
TP14
Vss
Vss
Vss
TP3
TN15
DLN4
Vdd
COMi1
COMi2
2
BLe
BLo
FIRST DATA CIRCUIT
SECOND DATA CIRCUIT
THIRD DATA CIRCUIT
FOURTH DATA CIRCUIT
FIFTH DATA CIRCUIT
SIXTH DATA CIRCUIT
SEVENTH DATA CIRCUIT
EIGHTH DATA CIRCUIT
REG2-0
REG2-1
REG2-2
REG2-3
REG2-0
REG2-1
REG2-2
REG2-3
I0j+0
nI0j+0
I0j+1
nI0j+1
I0j+2
nI0j+2
I0j+3
nI0j+3
I0j+4
nI0j+4
I0j+5
nI0j+5
I0j+6
nI0j+6
I0j+7
nI0j+7

FIG. 12



RMAINi : i-TH WORD LINE DRIVER
RADDi : i-TH ROW ADDRESS DECODER
RDECADSi : WORD LINE DRIVER SELECTING SIGNAL
i=1.2.3.4. • • •

FIG. 13

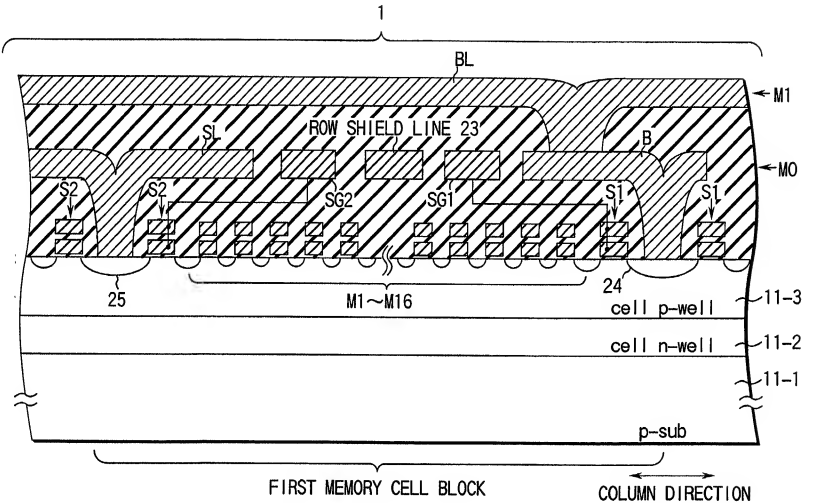


FIG. 14

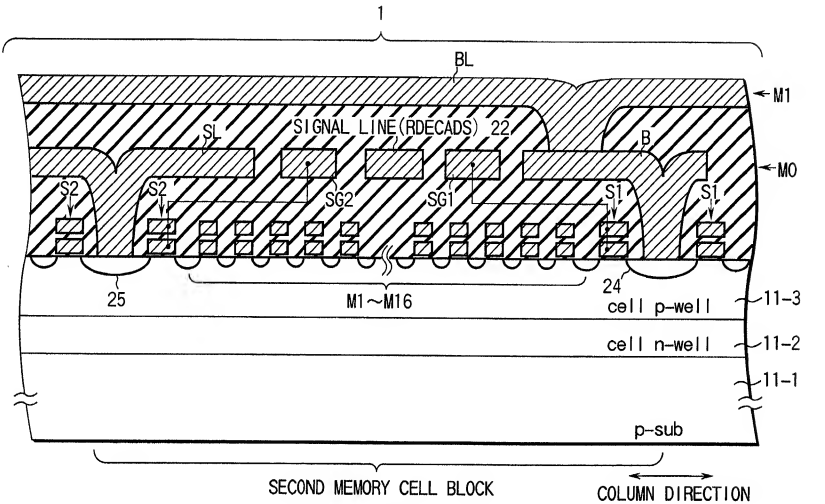


FIG. 15

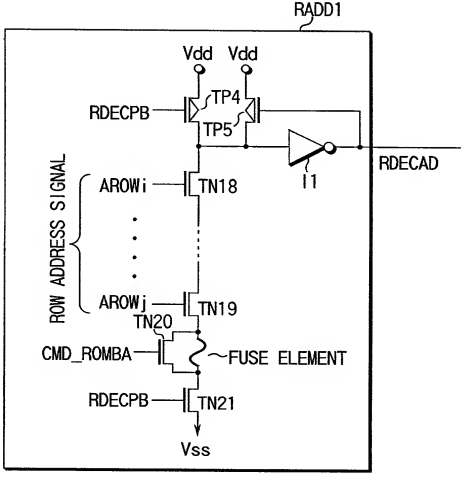


FIG. 16

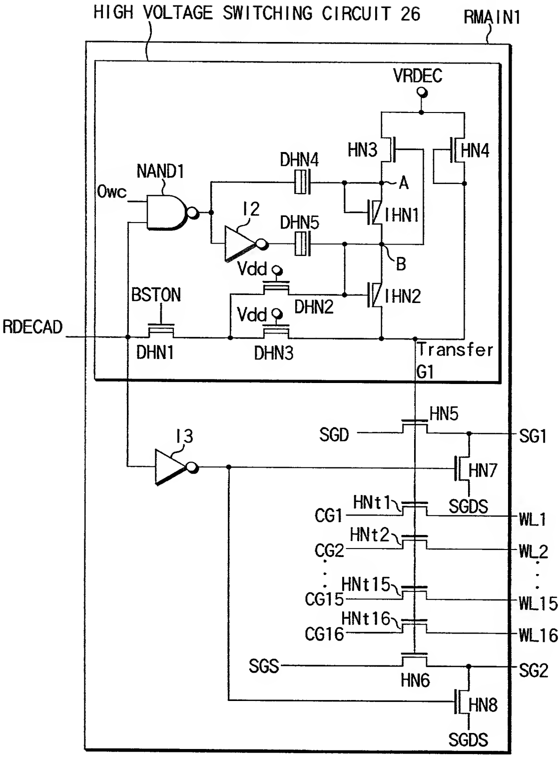

HIGH VOLTAGE SWITCHING CIRCUIT 26
RMAIN1
VRDEC
HN3
HN4
DHN4
NAND1
Owc
A
I2
DHN5
IHN1
B
Vdd
BSTON
IHN2
DHN2
Vdd
RDECAD
DHN1
DHN3
Transfer
G1
HN5
SGD
SG1
I3
HN7
HNt1
SGDS
CG1
WL1
HNt2
CG2
WL2
HNt15
CG15
WL15
HNt16
CG16
WL16
SGS
SG2
HN6
HN8
SGDS

FIG. 17

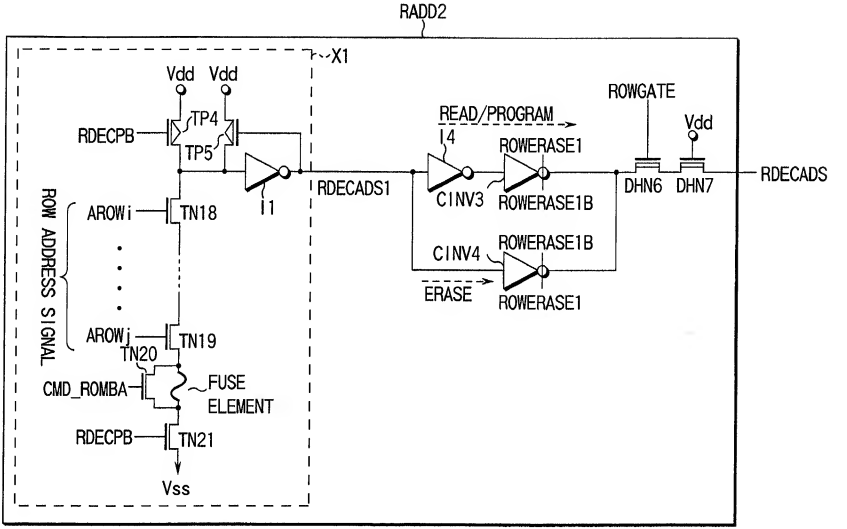


FIG. 18

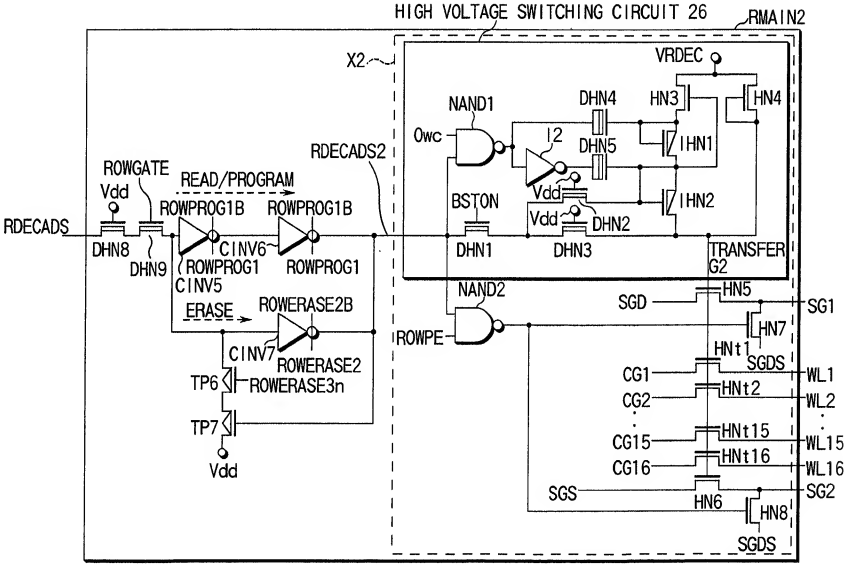

HIGH VOLTAGE SWITCHING CIRCUIT 26
RMAIN2
X2
VRDEC
NAND1
DHN4
HN3
HN4
Owc
I2
DHN5
IHN1
IHN2
Vdd
BSTON
DHN2
DHN1
DHN3
TRANSFER G2
RDECADS2
ROWGATE
READ/PROGRAM
RDECADS
DHN8
DHN9
ROWPROG1B
ROWPROG1B
CINV6
ROWPROG1
ROWPROG1
CINV5
ERASE
ROWERASE2B
CINV7
ROWERASE2
TP6
ROWERASE3n
TP7
Vdd
NAND2
ROWPE
SGD
HN5
SG1
HN7
HNt1
SGDS
CG1
HNt2
WL1
CG2
WL2
CG15
HNt15
WL15
CG16
HNt16
WL16
SGS
HN6
HN8
SG2
SGDS

FIG. 19

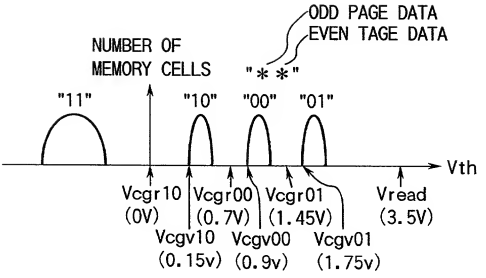


FIG. 20

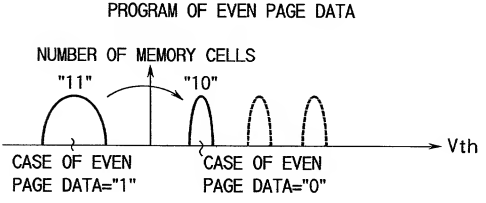


FIG. 21

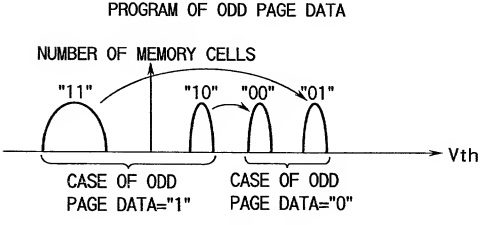


FIG. 22

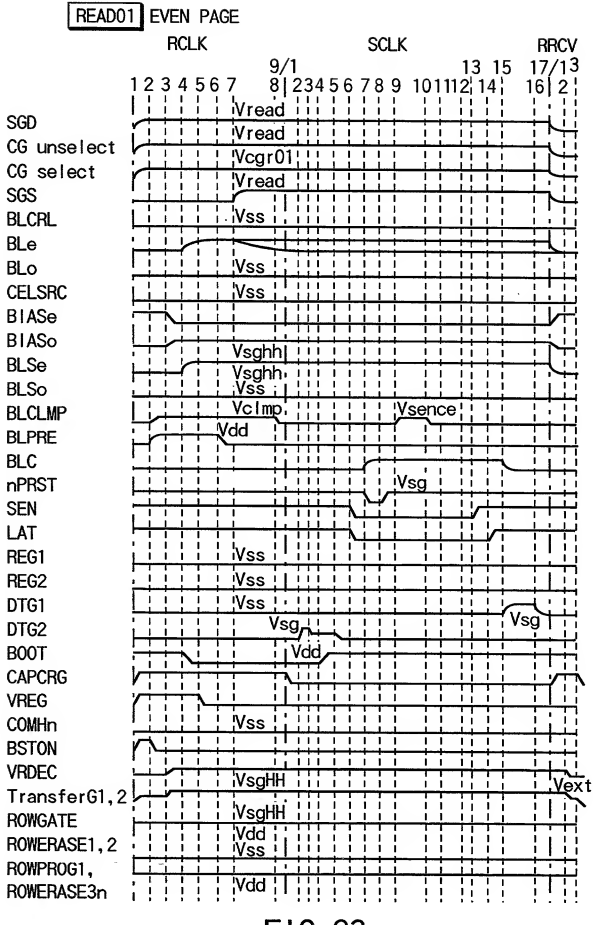


FIG. 23

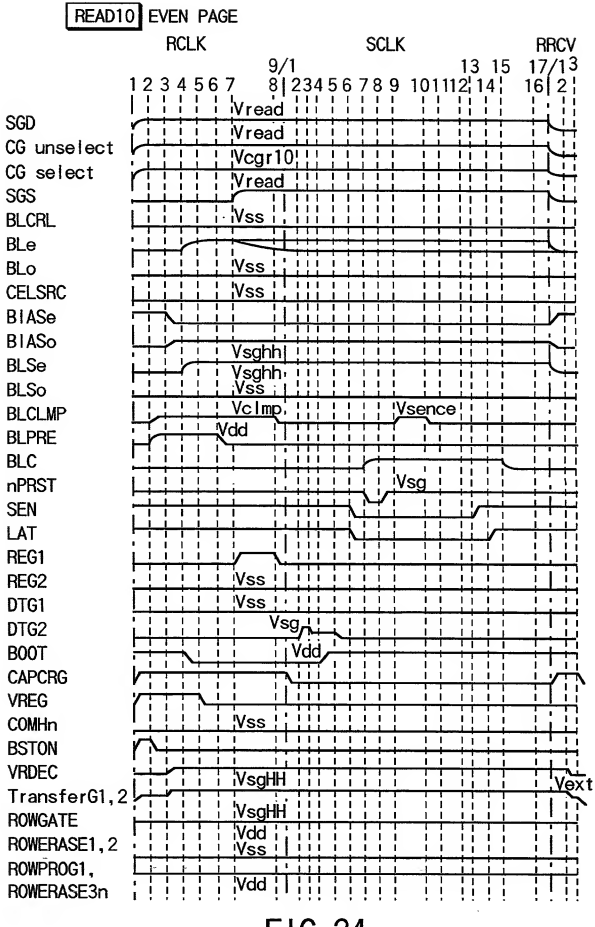

READ10 EVEN PAGE
RCLK
SCLK
RRCV
9/1
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17/1 2 3
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgr10
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 24

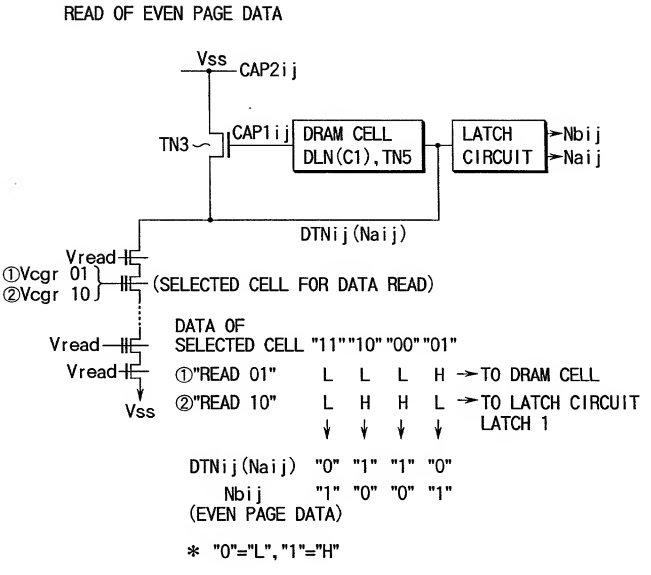


FIG. 25

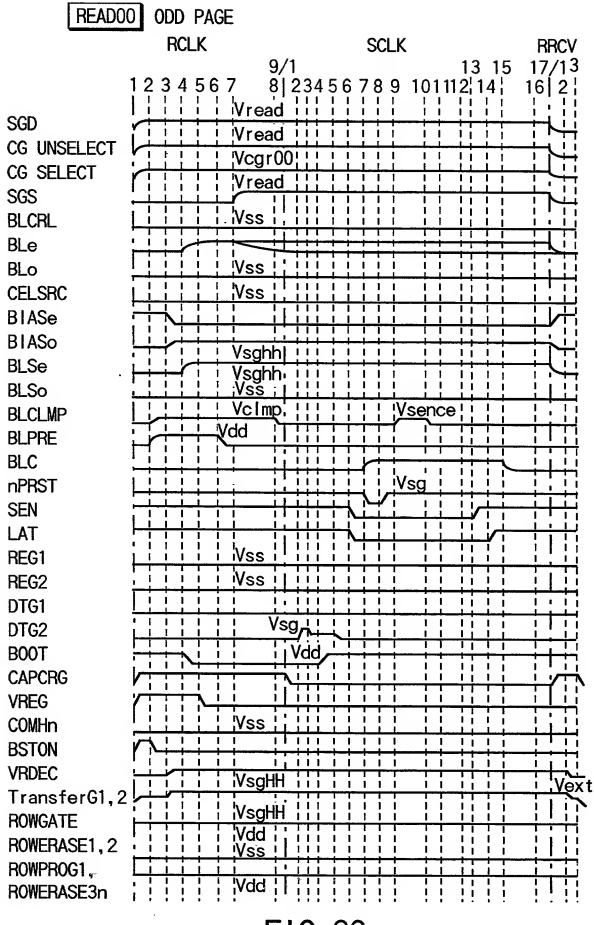

READ00
ODD PAGE
RCLK
SCLK
RRCV
9/1
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17/13 2
SGD
CG UNSELECT
CG SELECT
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgr00
Vss
Vsghh
Vclmp.
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 26

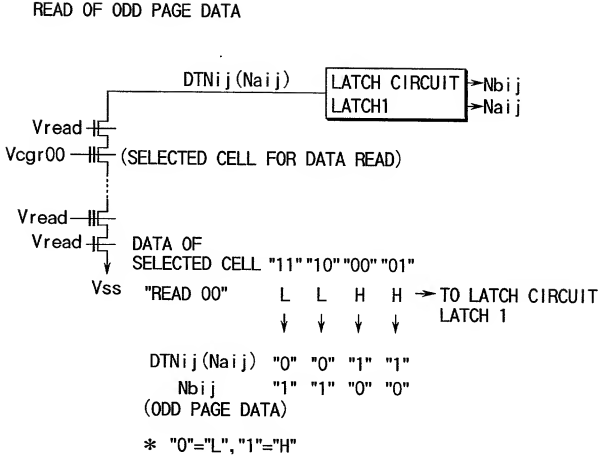

READ OF ODD PAGE DATA
DTNij(Naij)
LATCH CIRCUIT
LATCH1
Nbij
Naij
Vread
Vcgr00
(SELECTED CELL FOR DATA READ)
Vread
Vread
DATA OF
SELECTED CELL "11" "10" "00" "01"
Vss
"READ 00"
L L H H
TO LATCH CIRCUIT
LATCH 1
DTNij(Naij) "0" "0" "1" "1"
Nbij "1" "1" "0" "0"
(ODD PAGE DATA)
* "0"="L","1"="H"

FIG. 27

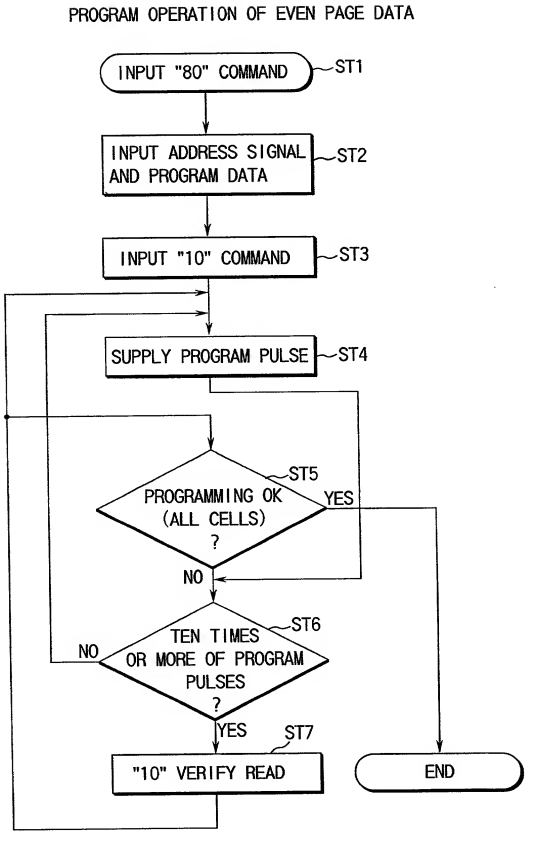

PROGRAM OPERATION OF EVEN PAGE DATA
INPUT "80" COMMAND
ST1
INPUT ADDRESS SIGNAL AND PROGRAM DATA
ST2
INPUT "10" COMMAND
ST3
SUPPLY PROGRAM PULSE
ST4
PROGRAMMING OK (ALL CELLS) ?
ST5
YES
NO
TEN TIMES OR MORE OF PROGRAM PULSES ?
ST6
NO
YES
"10" VERIFY READ
ST7
END

FIG. 28

PROGRAM WHEN LSB,WLs NEIGHBORING SELECTED WL SET Vss
PROGRAM COMPLETION DETECTION IS OPERATED TOO
IN PERIOD CCLK1～10

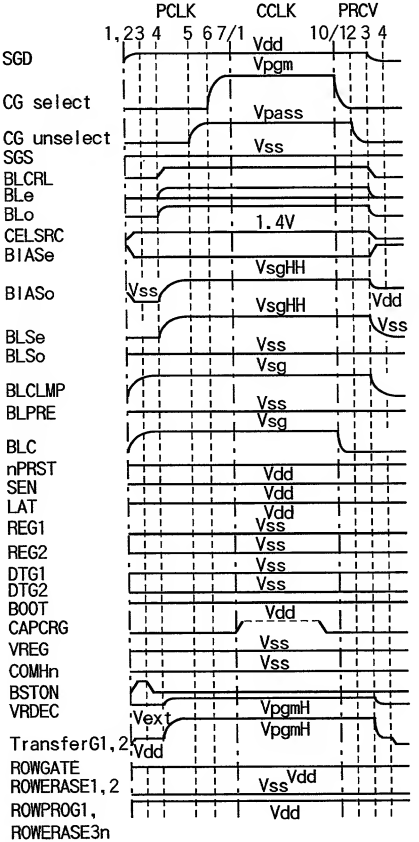


FIG. 29

PROGRAM OF EVEN PAGE DATA (SUPPLY PROGRAM PULSE)

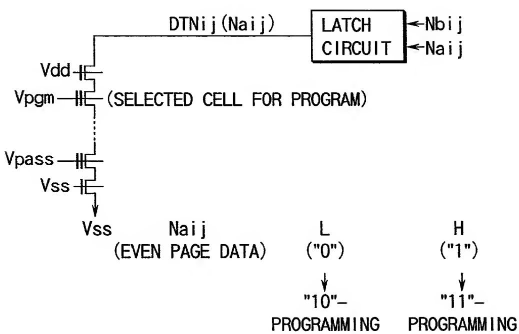


FIG. 30

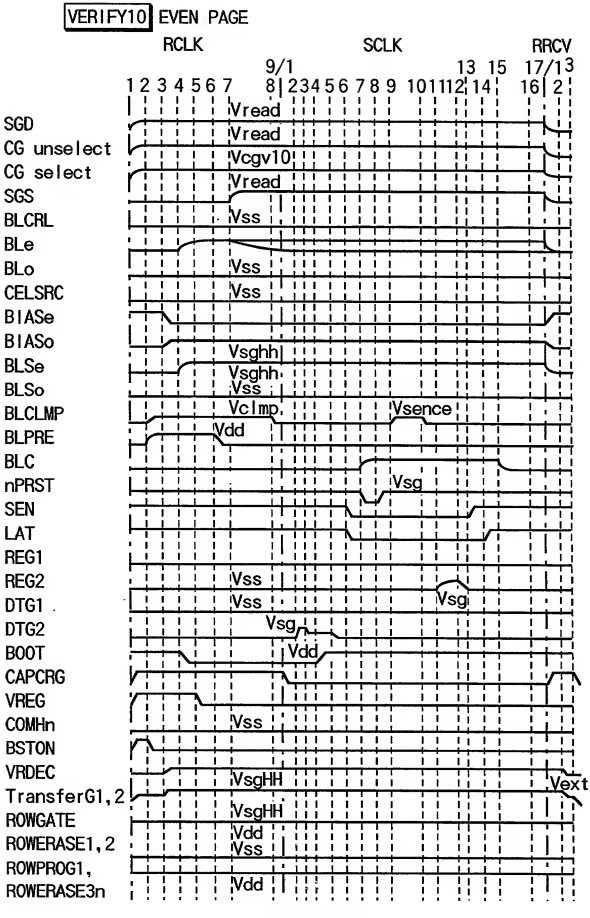
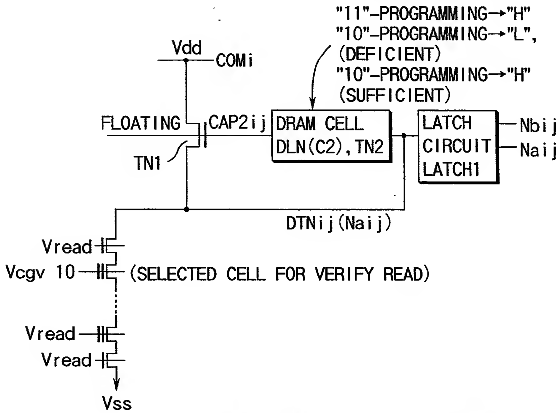

VERIFY10 EVEN PAGE
RCLK
SCLK
RRCV
9/1
13 15 17/13
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 14 16 2
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgv10
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 31

PROGRAM OF EVEN PAGE DATA ("10" VERIFY READ)



	"11"-PROGRAMMING	"10"-PROGRAMMING	
STATE OF SELECTED CELL	"11"	"10"DEFICIENT	"10"SUFFICIENT
BIT LINE	L	L	H
DTNij(Naij)	H	L	H → TO LATCH CIRCUIT LATCH1

FIG. 32

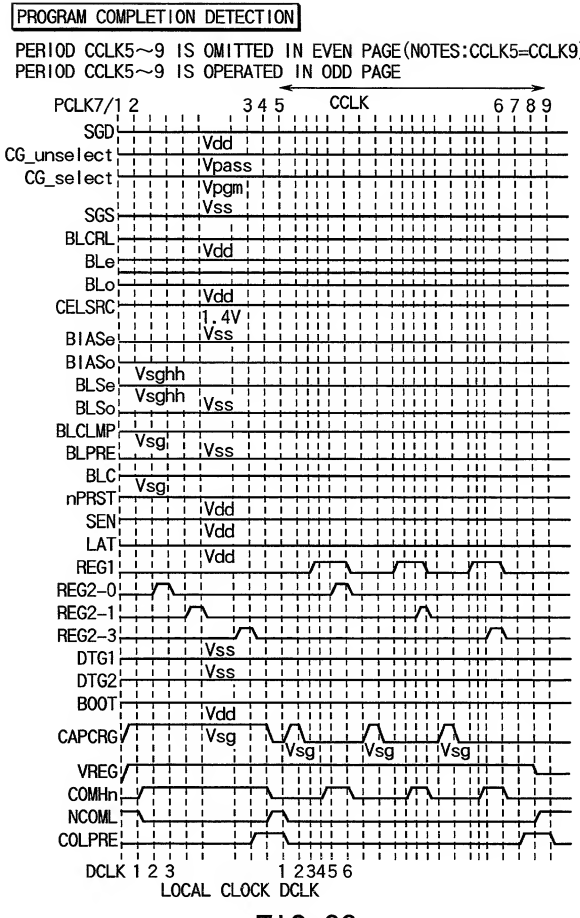

PROGRAM COMPLETION DETECTION
PERIOD CCLK5~9 IS OMITTED IN EVEN PAGE(NOTES:CCLK5=CCLK9)
PERIOD CCLK5~9 IS OPERATED IN ODD PAGE
PCLK7/1 2 3 4 5 CCLK 6 7 8 9
SGD
CG_unselect
CG_select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2-0
REG2-1
REG2-3
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
NCOML
COLPRE
Vdd
Vpass
Vpgm
Vss
1.4V
Vsghh
Vsg
DCLK 1 2 3 1 2 3 4 5 6
LOCAL CLOCK DCLK

FIG. 33

PROGRAM OF EVEN PAGE DATA (PROGRAM COMPLETION DETECTION)

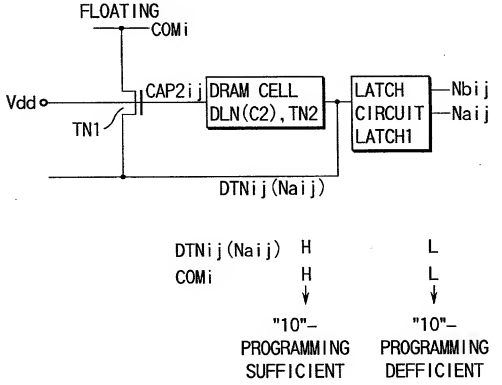


FIG. 34

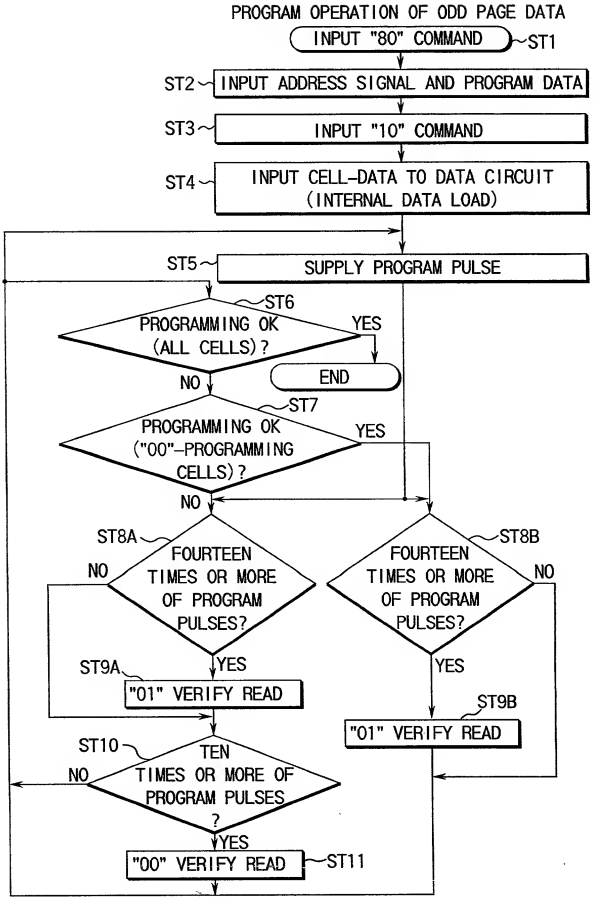

PROGRAM OPERATION OF ODD PAGE DATA
INPUT "80" COMMAND
ST1
ST2
INPUT ADDRESS SIGNAL AND PROGRAM DATA
ST3
INPUT "10" COMMAND
ST4
INPUT CELL-DATA TO DATA CIRCUIT (INTERNAL DATA LOAD)
ST5
SUPPLY PROGRAM PULSE
ST6
PROGRAMMING OK (ALL CELLS)?
YES
END
NO
ST7
PROGRAMMING OK ("00"-PROGRAMMING CELLS)?
YES
NO
ST8A
FOURTEEN TIMES OR MORE OF PROGRAM PULSES?
NO
YES
ST8B
FOURTEEN TIMES OR MORE OF PROGRAM PULSES?
NO
YES
ST9A
"01" VERIFY READ
ST9B
"01" VERIFY READ
ST10
TEN TIMES OR MORE OF PROGRAM PULSES ?
NO
YES
"00" VERIFY READ
ST11

FIG. 35

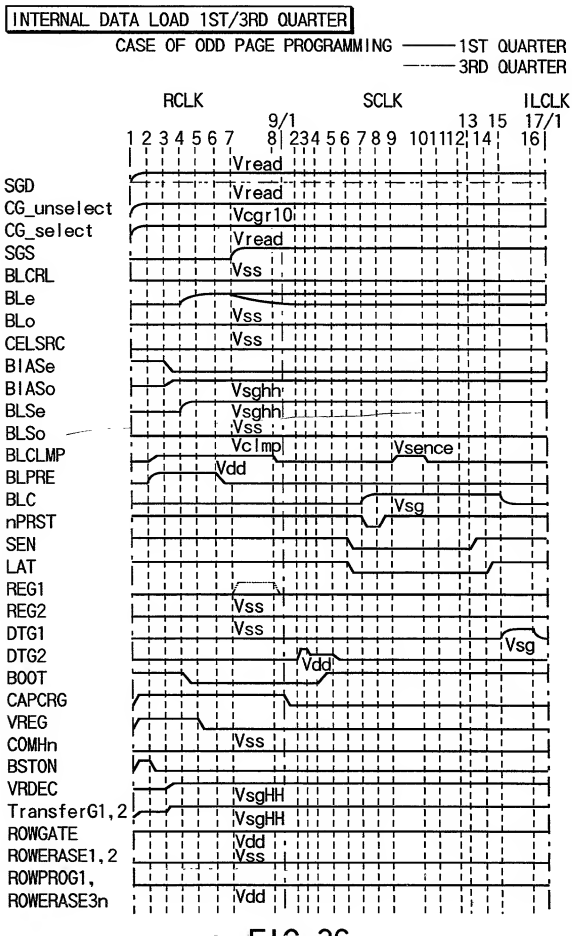
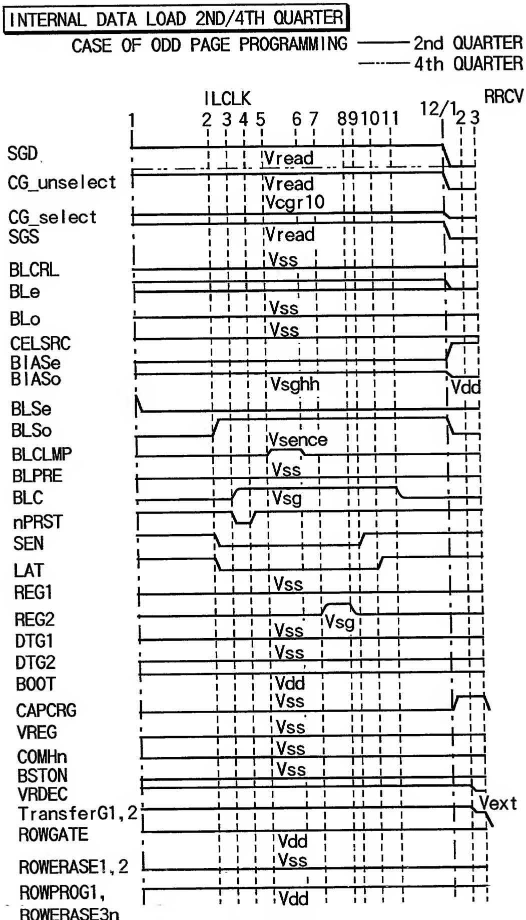

INTERNAL DATA LOAD 1ST/3RD QUARTER
CASE OF ODD PAGE PROGRAMMING
1ST QUARTER
3RD QUARTER
RCLK
SCLK
ILCLK
9/1
13 15 17/1
1 2 3 4 5 6 7 8 23 4 5 6 7 8 9 10 11 12 14 16
SGD
CG_unselect
CG_select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgr10
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH

FIG. 36


INTERNAL DATA LOAD 2ND/4TH QUARTER
CASE OF ODD PAGE PROGRAMMING
2nd QUARTER
4th QUARTER
ILCLK
1
2 3 4 5
6 7
891011
12/1
2 3
RRCV
SGD
CG_unselect
CG_select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vread
Vcgr10
Vread
Vss
Vss
Vss
Vsghh
Vdd
Vsence
Vss
Vsg
Vss
Vsg
Vss
Vss
Vdd
Vss
Vss
Vss
Vss
Vext
Vdd
Vss
Vdd
FIG. 37

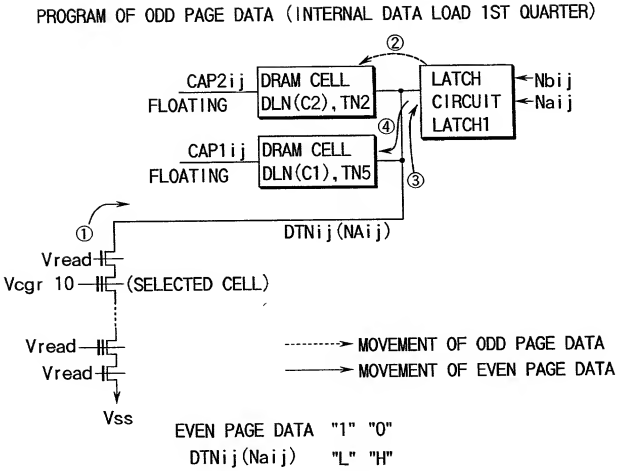
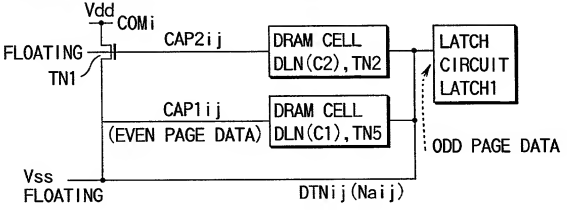


FIG. 38

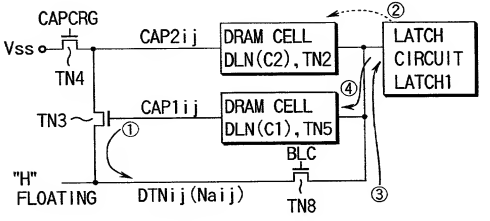
PROGRAM OF ODD PAGE DATA (INTERNAL DATA LOAD 2ND QUARTER)



ODD PAGE DATA	"1"	"0"
CAP2ij	"H"	"L"
DTNij	"H"	"L"
EVEN PAGE DATA	"1"	"0"
CAP1ij	"L"	"H"

FIG. 39

PROGRAM OF ODD PAGE DATA (INTERNAL DATA LOAD 3RD QUARTER)



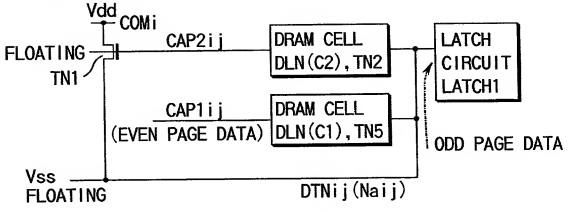
EVEN PAGE DATA	"1"	"0"
CAP1ij	"L"	"H"
DTNij	"H"	"L"

----------→ MOVEMENT OF ODD PAGE DATA

——————→ MOVEMENT OF EVEN PAGE DATA

FIG. 40

PROGRAM OF ODD PAGE DATA (INTERNAL DATA LOAD 4TH QUARTER)



ODD PAGE DATA	"1"	"0"
CAP2ij	"H"	"L"
DTNij	"H"	"L"
EVEN PAGE DATA	"1"	"0"
CAP1ij	"H"	"L"

FIG. 41

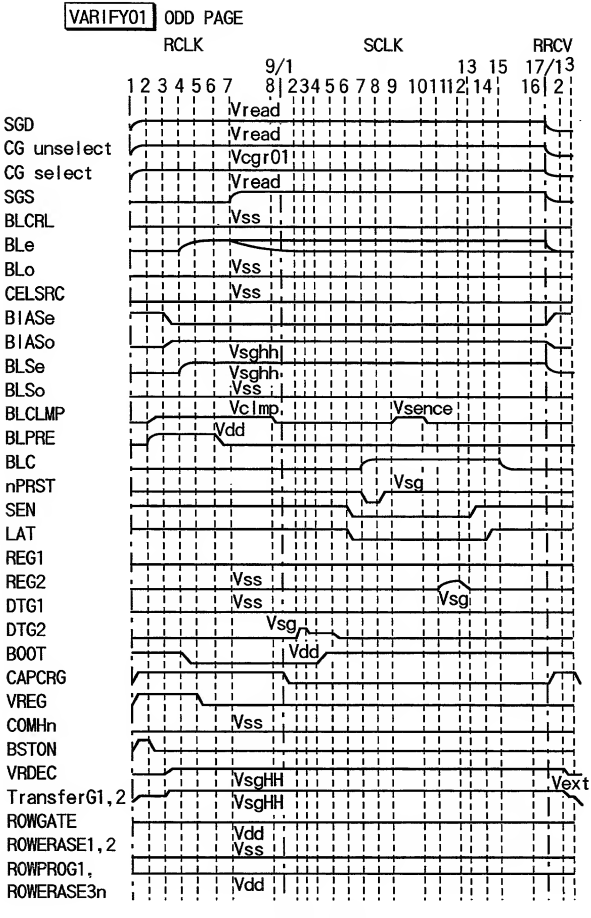
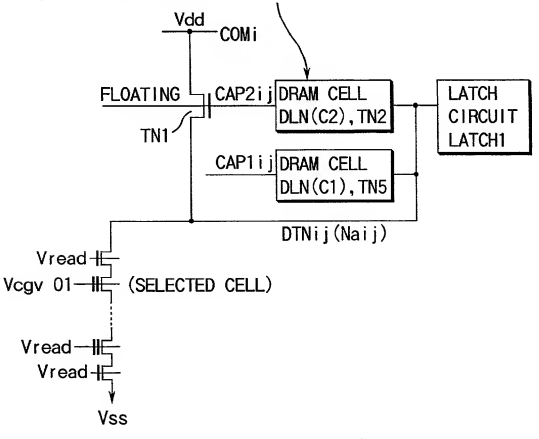

VARIFY01
ODD PAGE
RCLK
SCLK
RRCV
9/1
13 15
17/13
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 14 16 2
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgr01
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 42

PROGRAM OF ODD PAGE DATA ("01" VERIFY READ)

- "11","10"–PROGRAMMING→"H"(ODD PAGE DATA "1")
- "00","01"–PROGRAMMING (DEFICIENT)→"L"(ODD PAGE DATA "0")
- "01"–PROGRAMMING (SUFFICIENT)→"H"(ODD PAGE DATA "0"→"1")

＊"00"–PROGRAMMING (SUFFICIENT)→"10"–PROGRAMMING (ODD PAGE DATA "0"→"1")



	"11","10"–PROGRAMMING	"00"–PROGRAMMING		"01"–PROGRAMMING	
STATE OF SELECTED CELL	"11","10"	"00" DEFICIENT	"00" SUFFICIENT	"01" DEFICIENT	"01" SUFFICIENT
BIT LINE	L	L	L	L	H
DTNij(Naij)	H	L	H	L	H

NO DATA CHANGE

CHANGE OF ODD PAGE DATA "0"→"1"

TO LATCH CIRCUIT LATCH1

FIG. 43

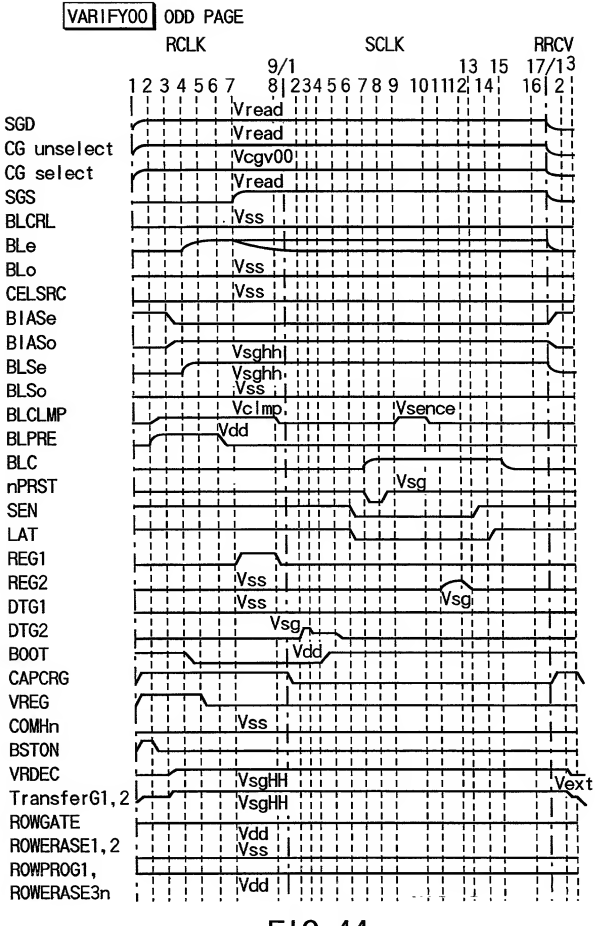
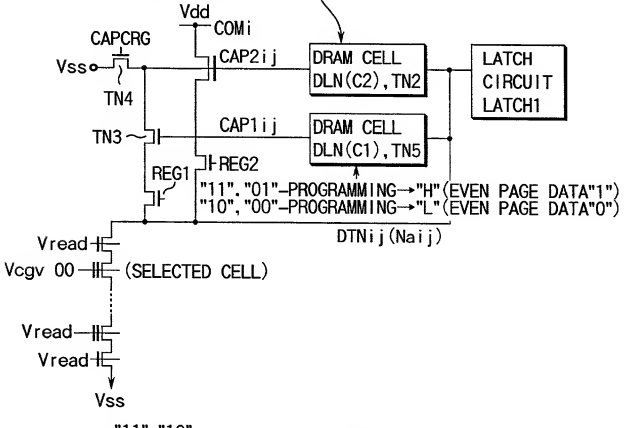

VARIFY00
ODD PAGE
RCLK
SCLK
RRCV
9/1
1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17/1 2 3
SGD
CG unselect
CG select
SGS
BLCRL
BLe
BLo
CELSRC
BIASe
BIASo
BLSe
BLSo
BLCLMP
BLPRE
BLC
nPRST
SEN
LAT
REG1
REG2
DTG1
DTG2
BOOT
CAPCRG
VREG
COMHn
BSTON
VRDEC
TransferG1,2
ROWGATE
ROWERASE1,2
ROWPROG1,
ROWERASE3n
Vread
Vcgv00
Vss
Vsghh
Vclmp
Vsence
Vdd
Vsg
VsgHH
Vext

FIG. 44

PROGRAM OF ODD PAGE DATA ("00" VERIFY READ)

- "11","10"-PROGRAMMING→"H"(ODD PAGE DATA "1")
- "00","01"-PROGRAMMING (DEFICIENT)→"L"(ODD PAGE DATA "0")
- "00"-PROGRAMMING (SUFFICIENT)→"H"(ODD PAGE DATA "0"→"1")

*"01"-PROGRAMMING (SUFFICIENT)→"11"-PROGRAMMING (ODD PAGE DATA "0"→"1")



	"11","10"-PROGRAMMING	"00"-PROGRAMMING		"01"-PROGRAMMING	
STATE OF SELECTED CELL	"11","10"	"00" DEFICIENT	"00" SUFFICIENT	"01" DEFICIENT	"01" SUFFICIENT
BIT LINE	L	L	H	H OR L	H
DTNij		↓	↓		
(PERIOD REG1="H")	L	L	H	L	L
DTNij		↓	↓		
(PERIOD REG2="H")	H	L	H	L	H
	NO DATA CHANGE		CHANGE OF ODD PAGE DATA "0"→"1"	NO DATA CHANGE	TO LATCH CIRCUIT LATCH1

FIG. 45

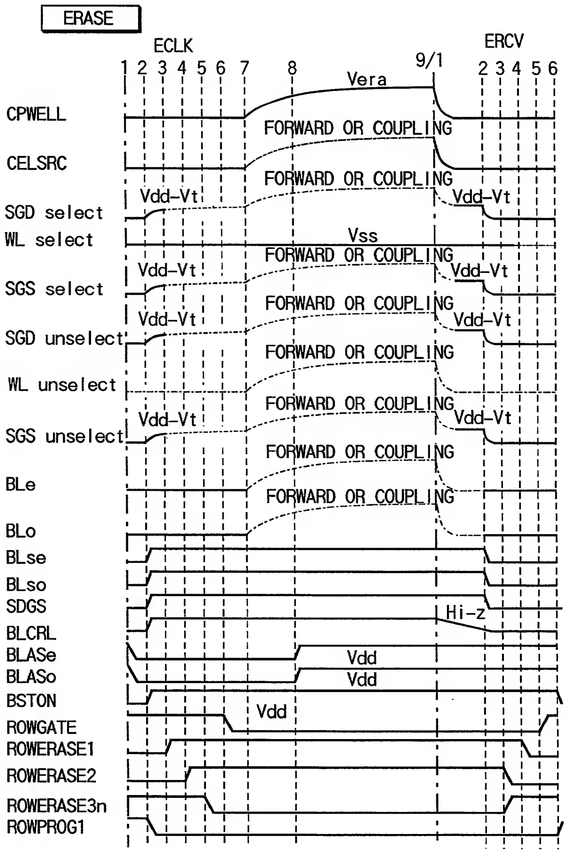

ERASE
ECLK
ERCV
1 2 3 4 5 6 7 8 9/1 2 3 4 5 6
Vera
CPWELL
FORWARD OR COUPLING
CELSRC
FORWARD OR COUPLING
Vdd-Vt
SGD select
WL select
Vss
FORWARD OR COUPLING
Vdd-Vt
SGS select
FORWARD OR COUPLING
Vdd-Vt
SGD unselect
FORWARD OR COUPLING
WL unselect
FORWARD OR COUPLING
Vdd-Vt
SGS unselect
FORWARD OR COUPLING
BLe
FORWARD OR COUPLING
BLo
BLse
BLso
SDGS
Hi-z
BLCRL
BLASe
Vdd
BLASo
Vdd
BSTON
Vdd
ROWGATE
ROWERASE1
ROWERASE2
ROWERASE3n
ROWPROG1

FIG. 46

ERASE VERIFY READ

VERIFY OF EVEN COLUMN→ALL DETECTION→DETECTION OF FAIL CELL NUMBER(Y-SCAN)→VERIFY OF ODD COLUMN→ALL DETECTION →DETECTION OF FAIL CELL NUMBER(Y-SCAN)

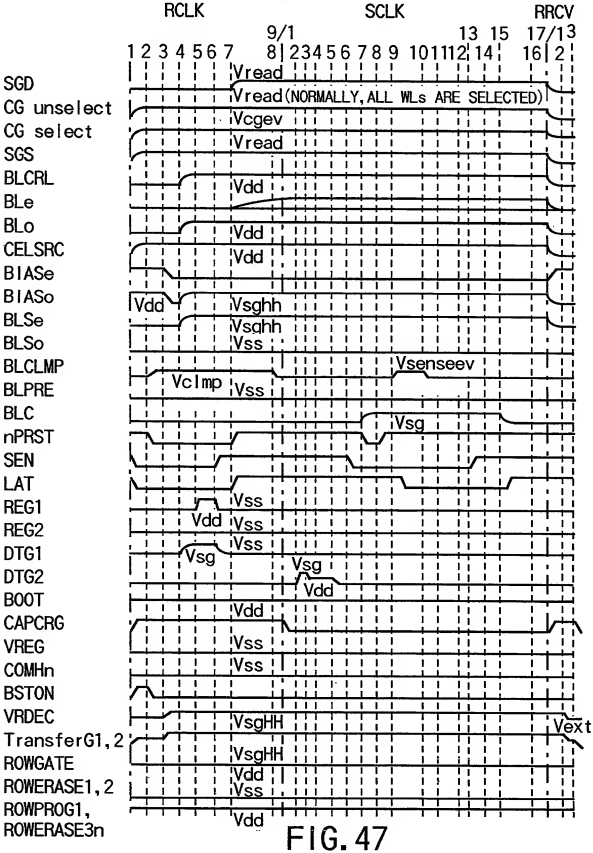


FIG. 47

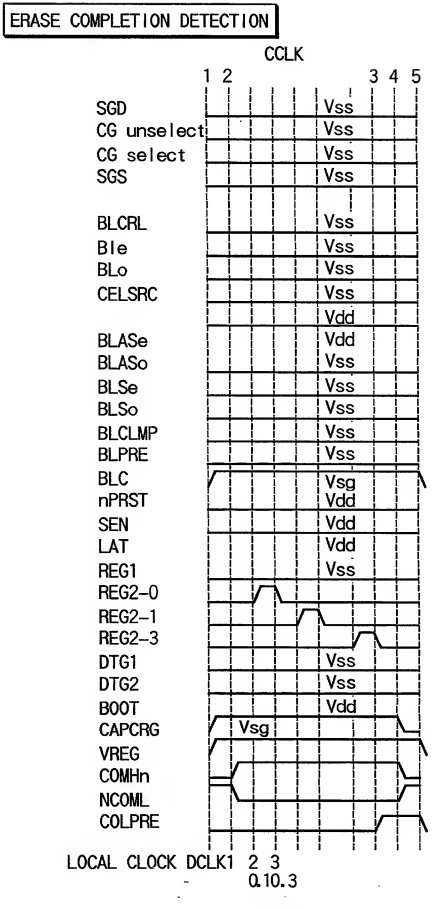


FIG. 48

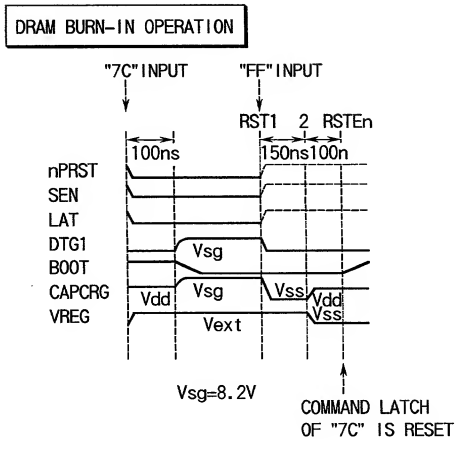

DRAM BURN-IN OPERATION
"7C" INPUT
"FF" INPUT
RST1
2
RSTEn
100ns
150ns
100n
nPRST
SEN
LAT
DTG1
BOOT
CAPCRG
VREG
Vsg
Vdd
Vsg
Vss
Vdd
Vss
Vext
Vsg=8.2V
COMMAND LATCH
OF "7C" IS RESET

FIG. 49

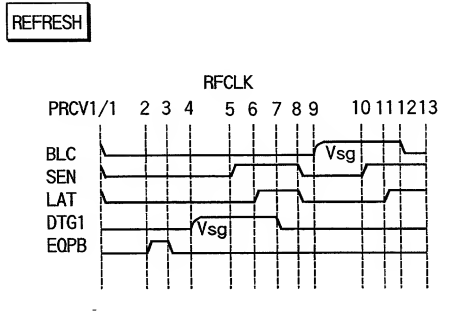

REFRESH
RFCLK
PRCV1/1
2 3 4
5 6 7 8 9
10 11 12 13
BLC
SEN
LAT
DTG1
EQPB
Vsg
Vsg

FIG. 50

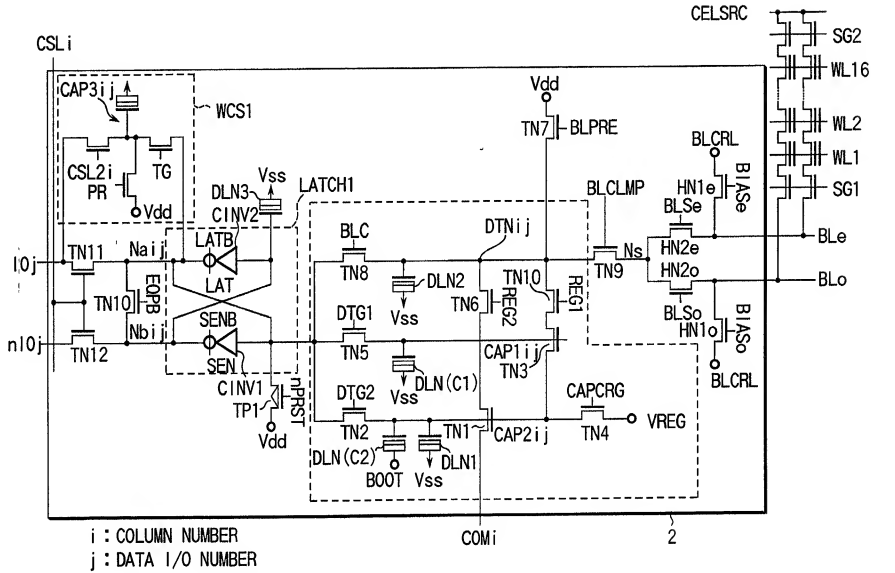


FIG. 51

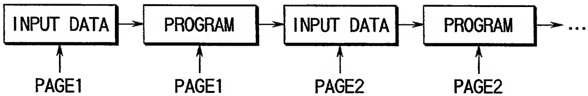

INPUT DATA
PROGRAM
INPUT DATA
PROGRAM
PAGE1
PAGE1
PAGE2
PAGE2

FIG. 52

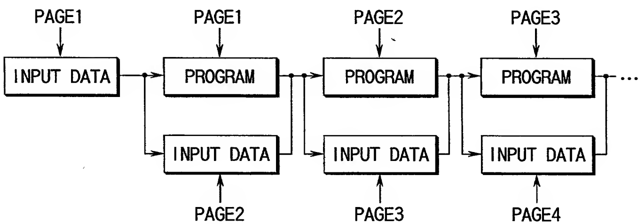

PAGE1
PAGE1
PAGE2
PAGE3
INPUT DATA
PROGRAM
PROGRAM
PROGRAM
INPUT DATA
INPUT DATA
INPUT DATA
PAGE2
PAGE3
PAGE4

FIG. 53

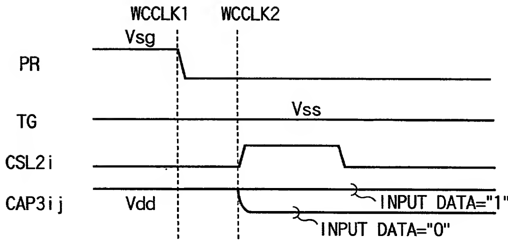

WCCLK1
WCCLK2
Vsg
PR
TG
Vss
CSL2i
CAP3ij
Vdd
INPUT DATA="1"
INPUT DATA="0"

FIG.54

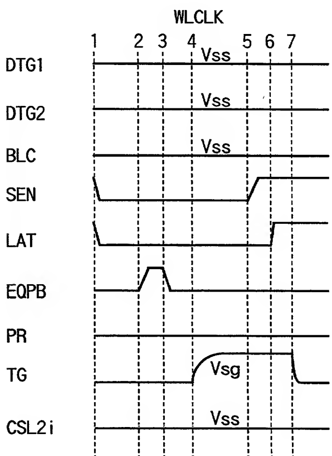

WLCLK
1 2 3 4 5 6 7
DTG1
Vss
DTG2
Vss
BLC
Vss
SEN
LAT
EQPB
PR
TG
Vsg
CSL2i
Vss

FIG.55

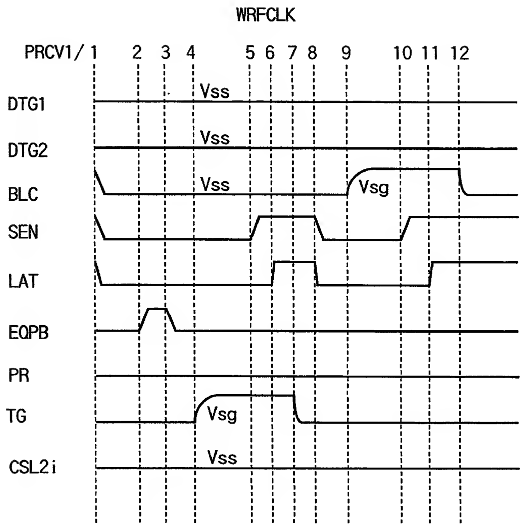

WRFCLK
PRCV1/ 1
2
3
4
5
6
7
8
9
10
11
12
DTG1
Vss
DTG2
Vss
BLC
Vss
Vsg
SEN
LAT
EQPB
PR
TG
Vsg
CSL2i
Vss

FIG. 56

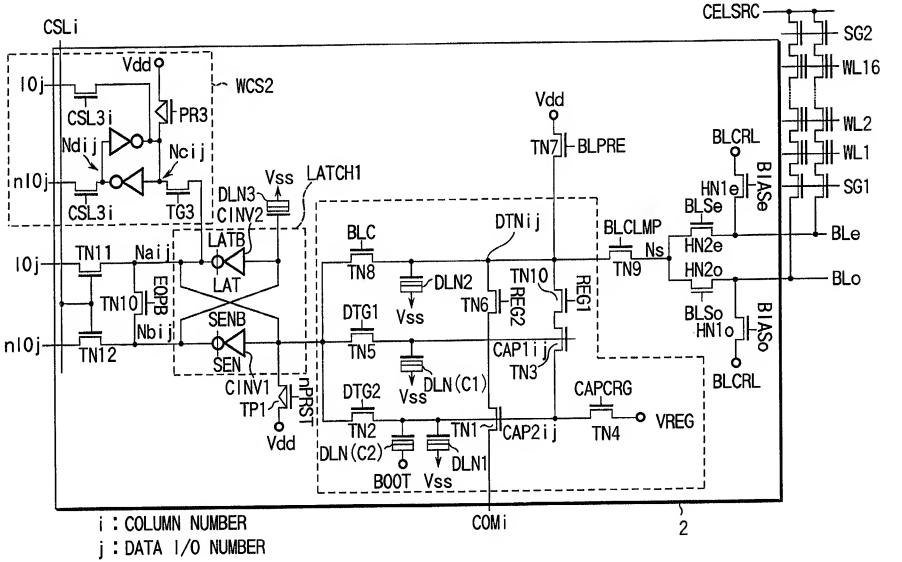


FIG. 57

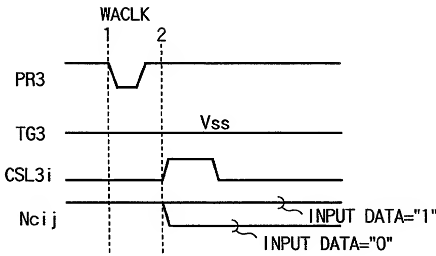

WACLK
1
2
PR3
TG3
Vss
CSL3i
Ncij
INPUT DATA="1"
INPUT DATA="0"

FIG. 58

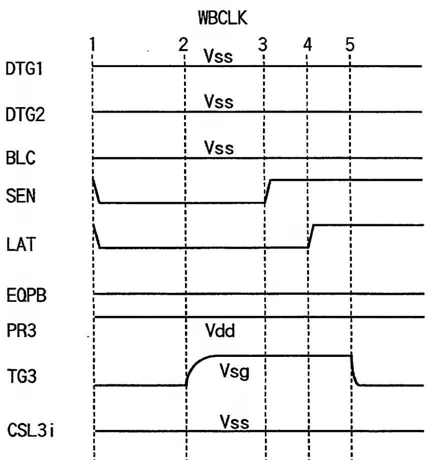

WBCLK
1
2
3
4
5
DTG1
Vss
DTG2
Vss
BLC
Vss
SEN
LAT
EQPB
PR3
Vdd
TG3
Vsg
CSL3i
Vss

FIG. 59

FIG. 60A

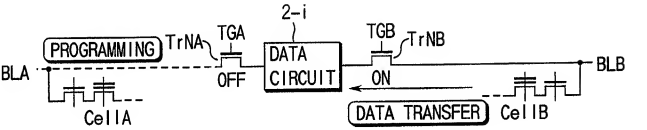


FIG. 60B

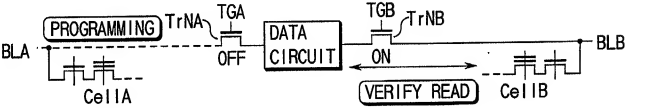


FIG. 60C

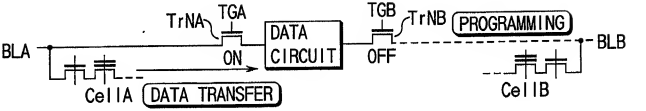
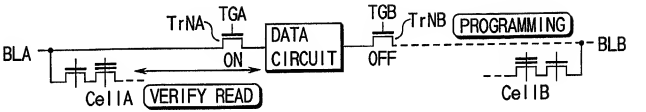


FIG. 60D



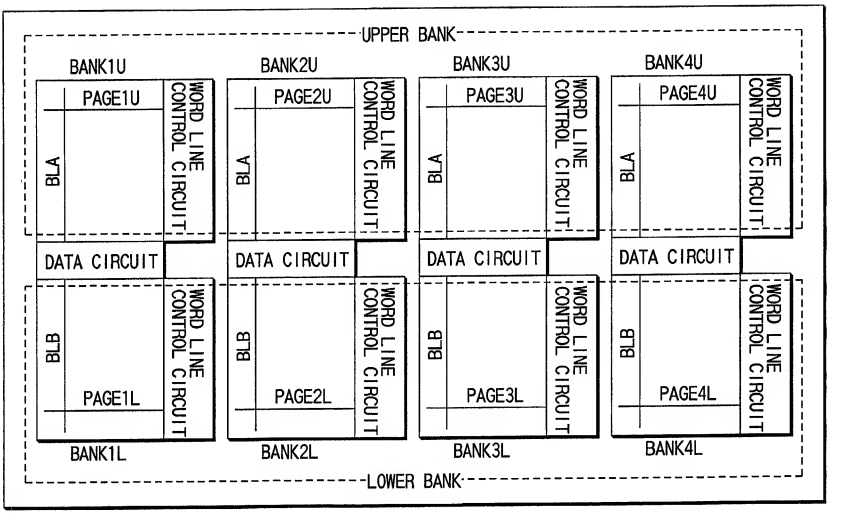


FIG. 61

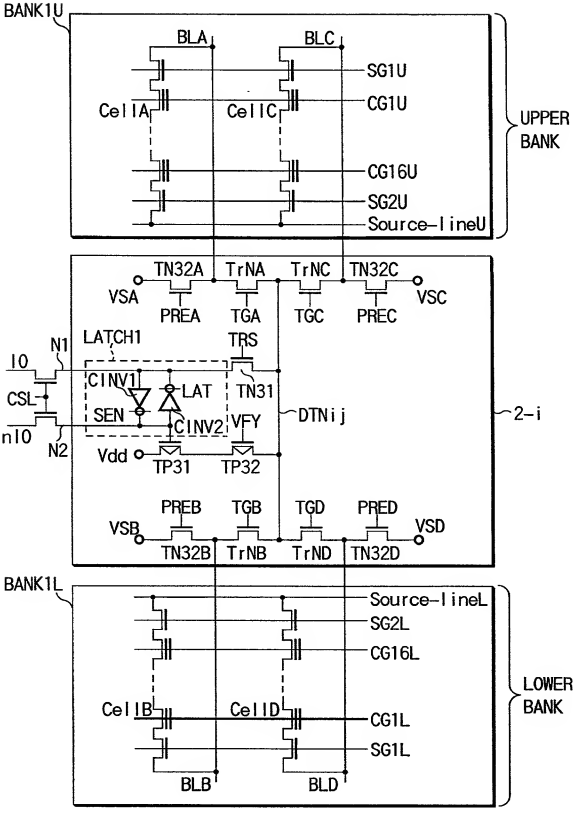

BANK1U
BLA
BLC
SG1U
CG1U
CellA
CellC
UPPER BANK
CG16U
SG2U
Source-lineU
TN32A
TrNA
TrNC
TN32C
VSA
VSC
PREA
TGA
TGC
PREC
N1
LATCH1
TRS
IO
CINV1
LAT
TN31
CSL
SEN
CINV2
VFY
DTNij
2-i
nIO
N2
Vdd
TP31
TP32
PREB
TGB
TGD
PRED
VSB
VSD
TN32B
TrNB
TrND
TN32D
BANK1L
Source-lineL
SG2L
CG16L
LOWER BANK
CellB
CellD
CG1L
SG1L
BLB
BLD

FIG. 62

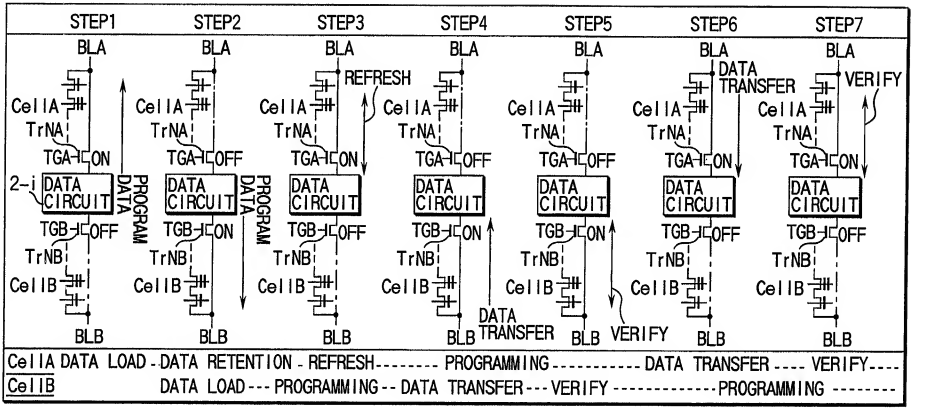


FIG. 63

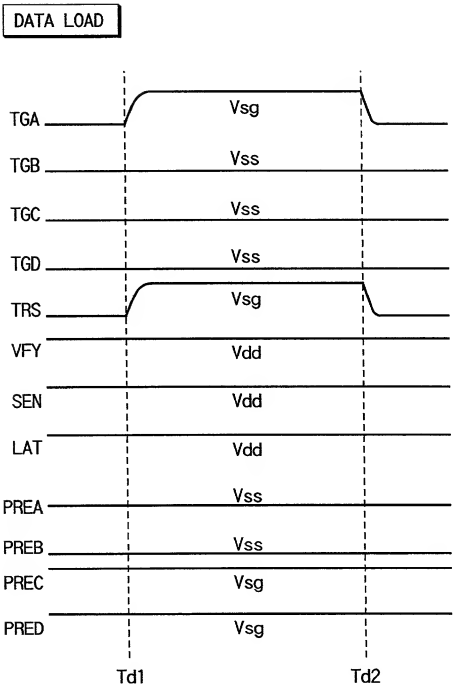

DATA LOAD
TGA
Vsg
TGB
Vss
TGC
Vss
TGD
Vss
TRS
Vsg
VFY
Vdd
SEN
Vdd
LAT
Vdd
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
Td1
Td2

FIG. 64

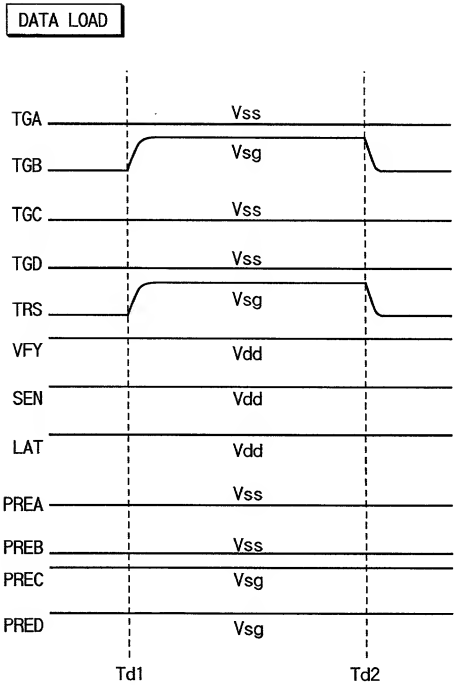


FIG. 65

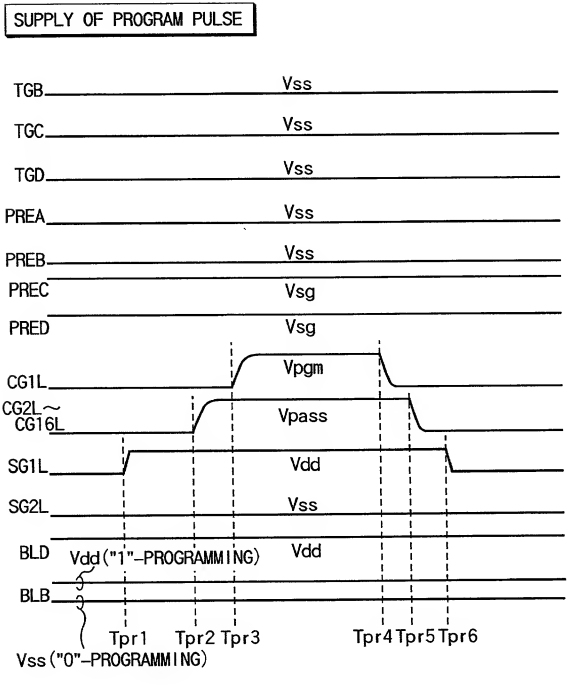


FIG. 66

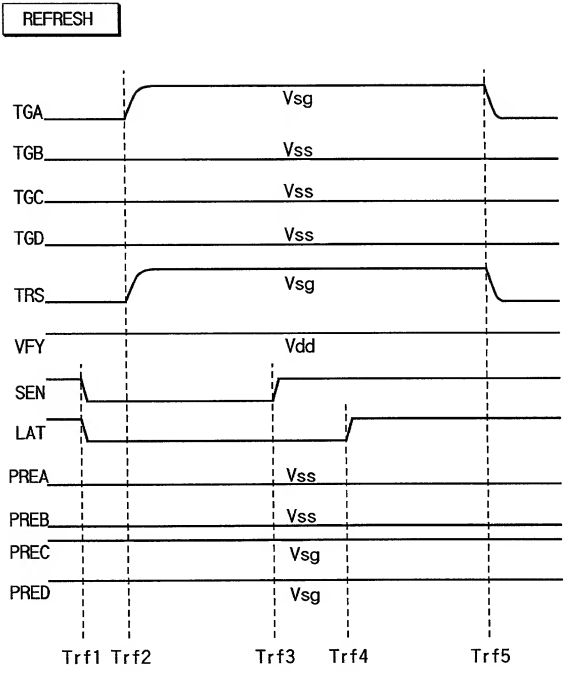


FIG. 67

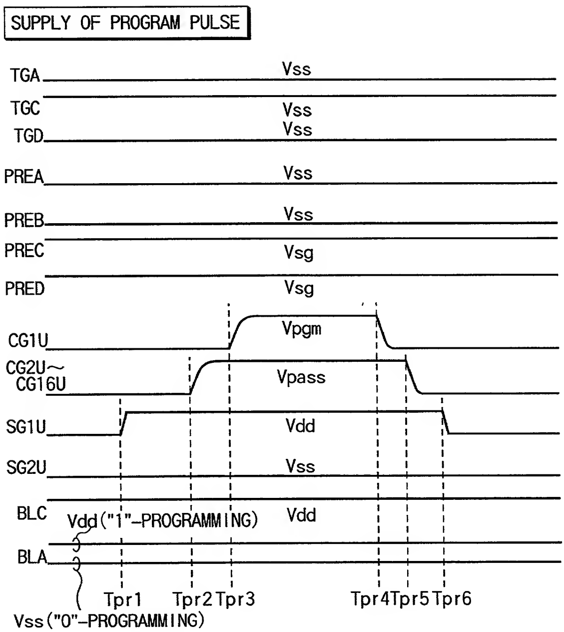

SUPPLY OF PROGRAM PULSE
TGA
Vss
TGC
Vss
TGD
Vss
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
CG1U
Vpgm
CG2U~
CG16U
Vpass
SG1U
Vdd
SG2U
Vss
BLC
Vdd
Vdd("1"-PROGRAMMING)
BLA
Tpr1
Tpr2
Tpr3
Tpr4
Tpr5
Tpr6
Vss("0"-PROGRAMMING)

FIG. 68

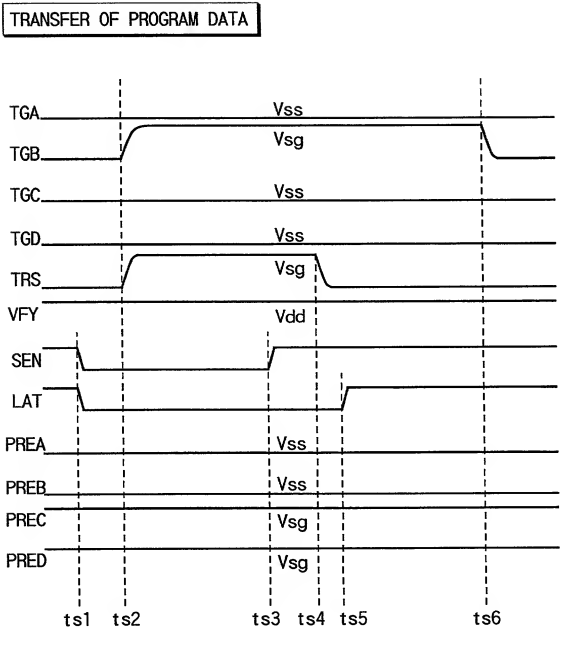


FIG. 69

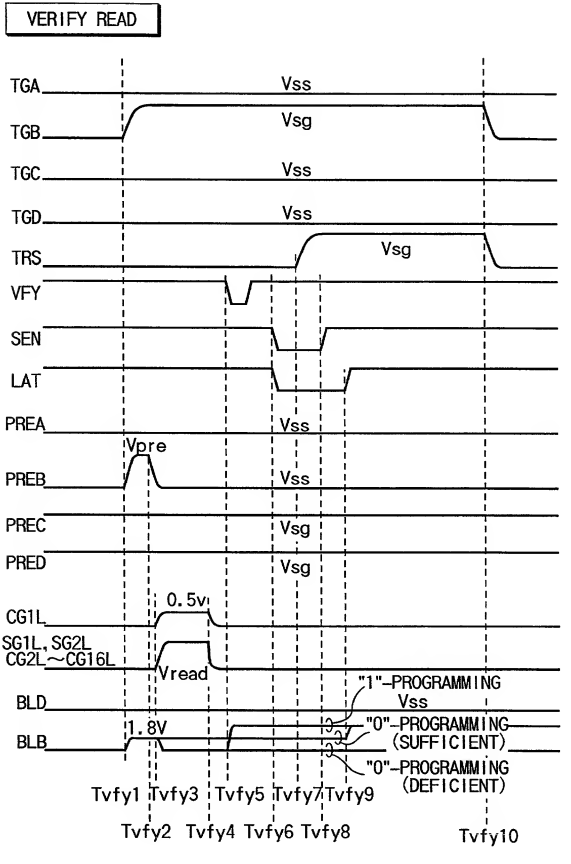

VERIFY READ
TGA
Vss
TGB
Vsg
TGC
Vss
TGD
Vss
TRS
Vsg
VFY
SEN
LAT
PREA
Vss
Vpre
PREB
Vss
PREC
Vsg
PRED
Vsg
0.5v
CG1L
SG1L, SG2L
CG2L~CG16L
Vread
"1"-PROGRAMMING
Vss
BLD
1.8V
"0"-PROGRAMMING
(SUFFICIENT)
BLB
"0"-PROGRAMMING
(DEFICIENT)
Tvfy1
Tvfy3
Tvfy5
Tvfy7
Tvfy9
Tvfy2
Tvfy4
Tvfy6
Tvfy8
Tvfy10

FIG. 70

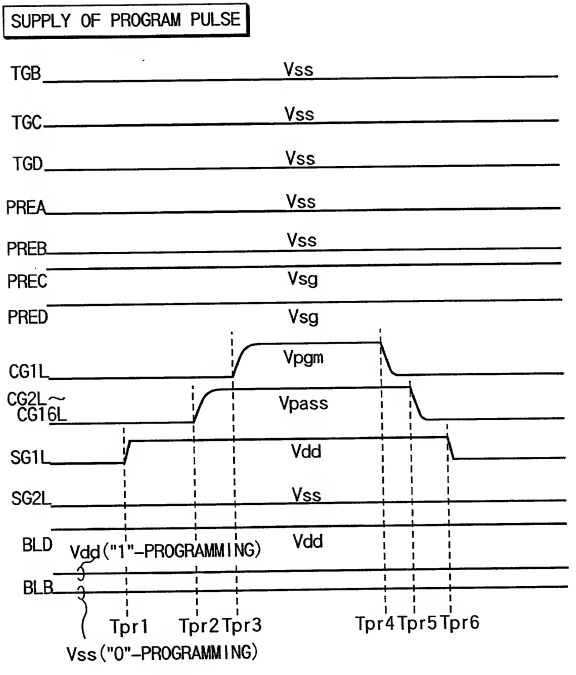

SUPPLY OF PROGRAM PULSE
TGB
Vss
TGC
Vss
TGD
Vss
PREA
Vss
PREB
Vss
PREC
Vsg
PRED
Vsg
CG1L
Vpgm
CG2L~
CG16L
Vpass
SG1L
Vdd
SG2L
Vss
BLD
Vdd("1"-PROGRAMMING)
Vdd
BLB
Vss("0"-PROGRAMMING)
Tpr1
Tpr2
Tpr3
Tpr4
Tpr5
Tpr6

FIG. 71

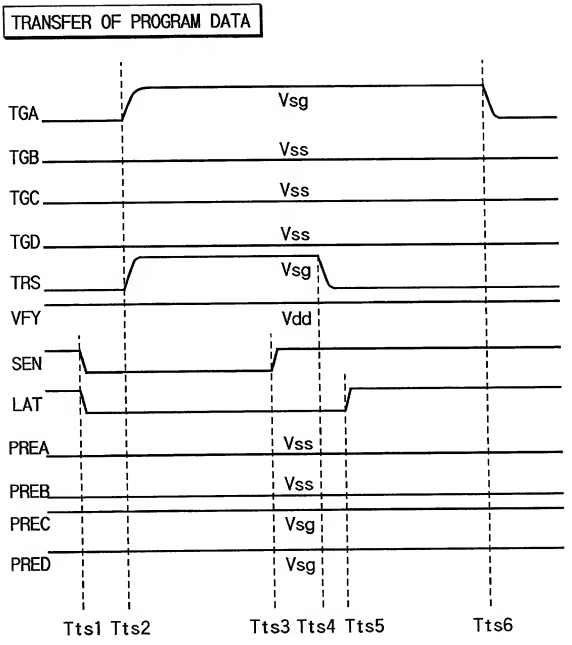


FIG. 72

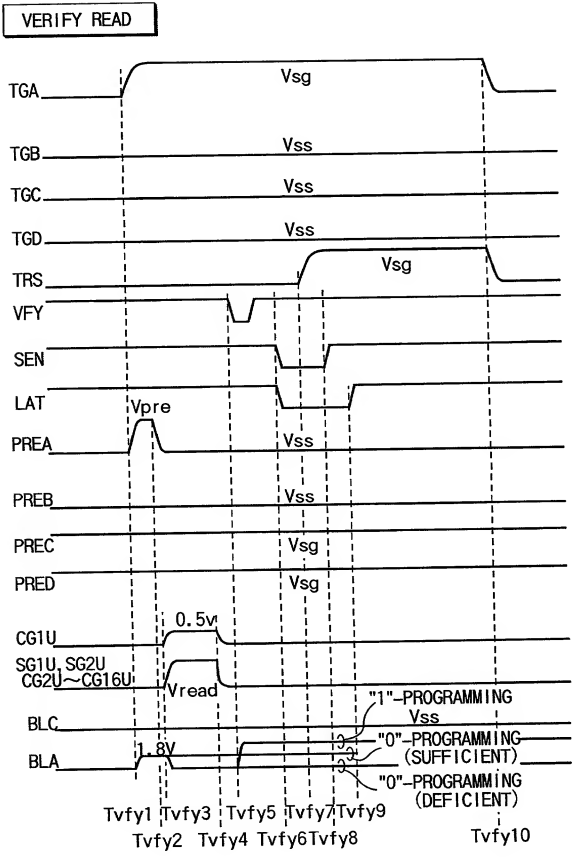


FIG. 73

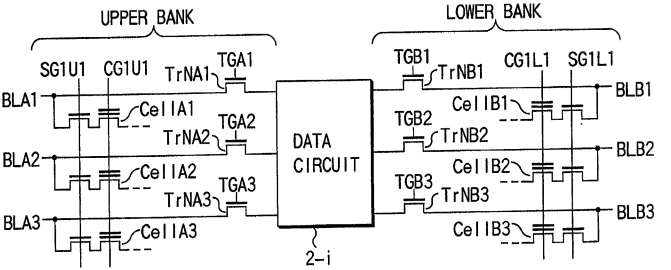


FIG. 74

	STEP1-1	STEP1-2	STEP1-3	STEP1-4	STEP1-5	STEP1-6	STEP1-7
TrNA1	ON	OFF	OFF	ON	OFF	OFF	OFF
TrNA2	OFF	ON	OFF	OFF	ON	ON	OFF
TrNA3	OFF	OFF	ON	OFF	OFF	OFF	OFF
TrNB1	OFF→ON	OFF	OFF	OFF→ON	OFF	OFF	ON
TrNB2	OFF	OFF→ON	OFF	OFF	OFF→ON	ON	OFF
TrNB3	OFF	OFF	OFF→ON	OFF	OFF	OFF	OFF
CellA1	DATA LOAD----	DATA RETENTION	-----REFRESH-------		PROGRAMMING---	DATA TRANSFER FROM BLB1 TO DL	
CellA2	——	DATA LOAD----	DATA RETENTION	---REFRESH--	PROGRAMMING---	DATA RETENTION	
CellA3	——	——	DATA LOAD----	DATA RETENTION	---PROGRAMMING---	DATA RETENTION	

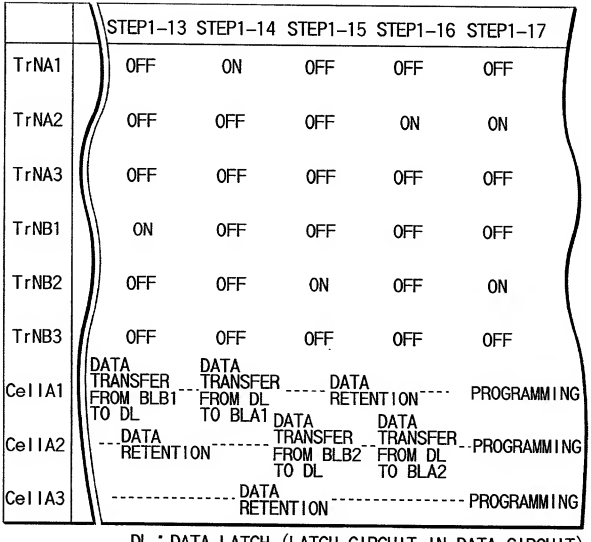
DL : DATA LATCH (LATCH CIRCUIT IN DATA CIRCUIT)

FIG. 75

	STEP1-8	STEP1-9	STEP1-10	STEP1-11	STEP1-12
TrNA1	ON	OFF	OFF	OFF	OFF
TrNA2	OFF	OFF	ON	OFF	OFF
TrNA3	OFF	OFF	OFF	OFF	ON
TrNB1	OFF→ON	OFF	OFF	OFF	OFF
TrNB2	OFF	ON	OFF→ON	OFF	OFF
TrNB3	OFF	OFF	OFF	ON	OFF→ON
CellA1	VERIFY ----------		DATA RETENTION ----------		
CellA2	DATA RETENTION --	DATA TRANSFER FROM BLB2 TO DL	-- VERIFY -------	DATA RETENTION	-----
CellA3	DATA RETENTION ----------			DATA TRANSFER FROM BLB3 TO DL	--- VERIFY

DL : DATA LATCH (LATCH CIRCUIT IN DATA CIRCUIT)

FIG. 76



DL : DATA LATCH (LATCH CIRCUIT IN DATA CIRCUIT)

FIG. 77

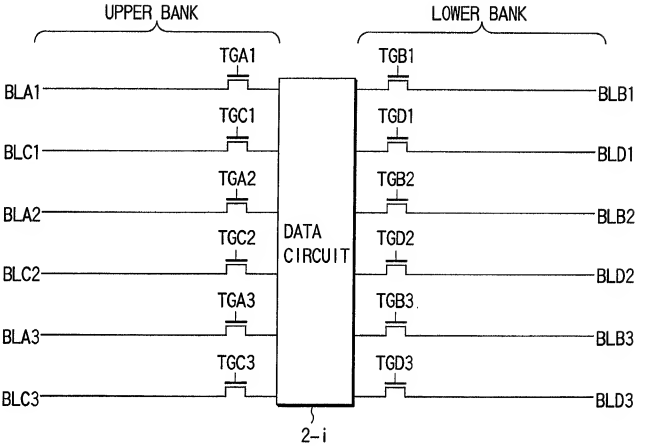


FIG. 78